MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 3, 2015/2016

EEN1046 – ELECTRONICS III

(All sections / Groups)

2 JUNE 2016
2.30 p.m. – 4.30 p.m.
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 5 pages with 4 Questions only excluding cover page.
2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is given.
3. Please write all your answers in the Answer Booklet provided.

Question 1

[A]

(i) Using an ideal op-amp, sketch an inverting amplifier circuit (with proper values of components) for voltage gain of -100 and input impedance of 10KΩ.

[5Marks]

(ii) Determine the output impedance of the circuit in part (i).

[1Mark]

[B] For the circuit as shown in Figure Q1[B], determine the output voltage. Assume op-amp is ideal. Take V_1=2V, V_2=3V, R_1=1KΩ,R_2=1KΩ, R_f=5KΩ and R_g=8KΩ.

[6Marks]

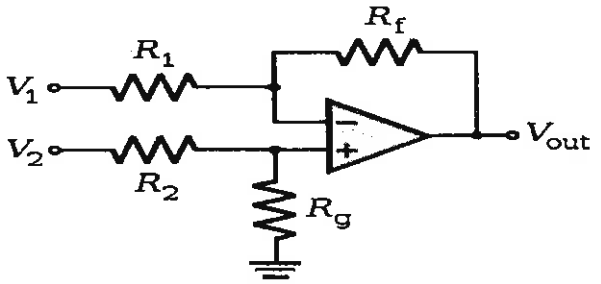

Figure Q 1[B]

[C] Sketch an inverting amplifier circuit at block level and circuit level, using ideal op-amp and diode, which gives output voltage

$$V_o=V_1 x V_2$$

Where; V_1 and V_2 are input voltages. The current through diode is given as

$i_D=10^{-3}[e^{Vd/1}-1]$ amp.

[4+6Marks]

[D] Sketch the output of the circuit as shown in Figure Q1[D] for the given input signal (V_{in}). Assume ideal op-amp.

[3Marks]

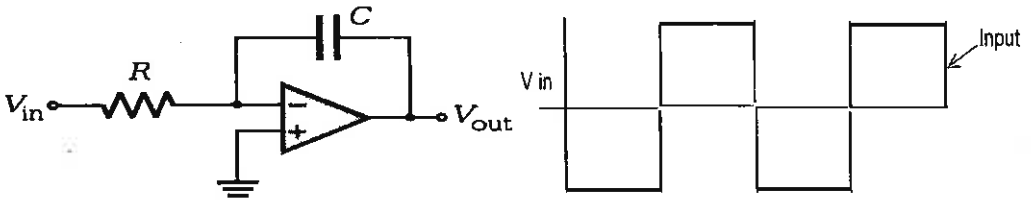

Figure Q1[D]

Continued .....

Question 2

[A] Consider an inverting op-amp configuration with R_1=1KΩ and R_2=100KΩ. Take open loop gain (A_{oL}) of the op-amp equal to 10^3, R_o=2Ω.

(i) Analyse the circuit in terms of closed voltage gain.

(ii) Determine the percentage gain error (PGE)

(iii)If open loop gain changes from 10^3 to 10^5, analyse the corresponding percentage change in the magnitude of the closed loop gain.

(iv)Determine the input and output impedances of the real op-amp used in this problem

[3+2+3+4 Marks]

[B] Evaluate the output voltage of the circuit as shown in Figure Q2[B] in terms of R_1 and R_2 when the op-amp has input offset voltage is V_{os}. The used op-amp is suffering only from offset voltage problem and is ideal in all other respects.

[6Marks]

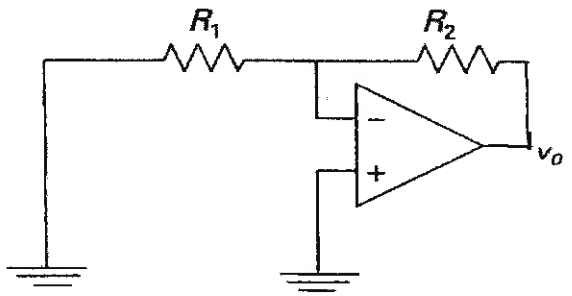

Figure Q2[B]

[C] Determine CMRR of the differential amplifier circuit as shown in Figure Q2[C]. Take V_1=2V, V_2=3V, R_1=1KΩ, R_2=1KΩ, R_f=5KΩ and R_g=8KΩ.

[7Marks]

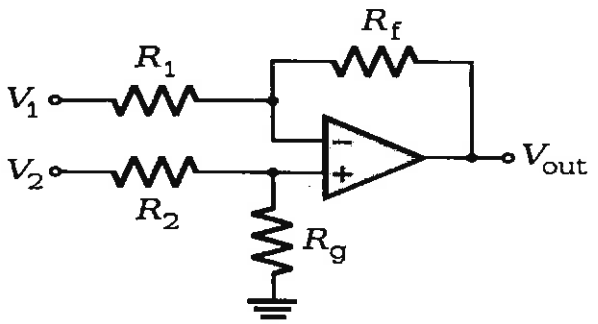

Figure Q2[C]

Continued .....

Question 3

[A] Sketch a low pass first order inverting filter using ideal op-amp with R_1=1KΩ and gain of 10. The cutoff frequency of the filter is 100Hz.

[5 Marks]

[B] The Darlington-pass transistor regulator circuit shown in Fig. Q3 [B] regulates the output voltage to 5V. Given that the transistor current gain for Q1 and Q2 are 100 and V_{BE} = 0.7V.

(i) Find the total Darlington-pair current gain, h_{FE}

[2 Marks]

(ii) Find the Zener voltage, V_Z and Zener current I_Z.

[6 Marks]

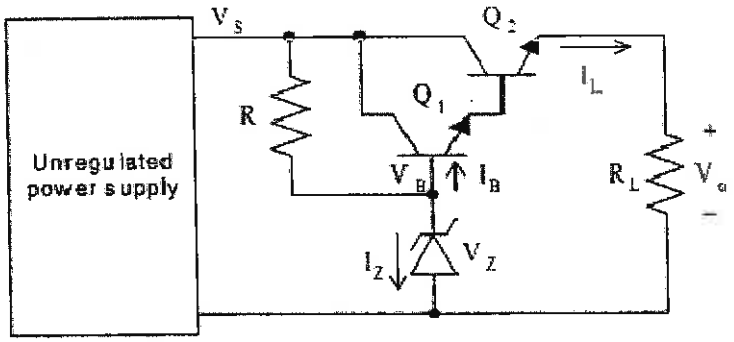

Fig. Q3 [B]

[C] Determine the inductor values in a Hartley oscillator shown in Fig. Q3[C]. The capacitance value C = 0.2 pF, Hartley oscillator frequency of oscillation (f_o) =5MHz and the feedback factor of oscillation (H) = 0.5.

[6 Marks]

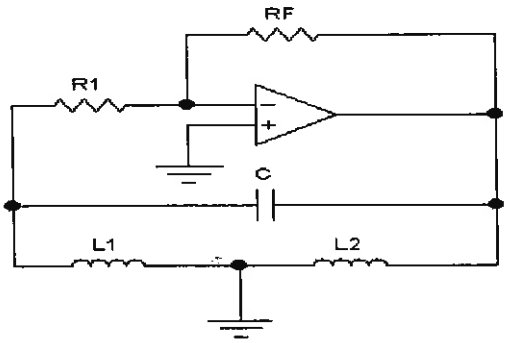

Fig.Q3[C]

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[D] The RC phase shift oscillator is shown in Fig. Q3 [D]. Determine the following:

i. Resonant frequency of an oscillator if R1=R2=R3=R=3kΩ and C1=C2=C3=C=4μF.

ii. Resistance(R) value if C=2pF and Oscillation frequency (f_o) = 500kHz

[3+3 Marks]

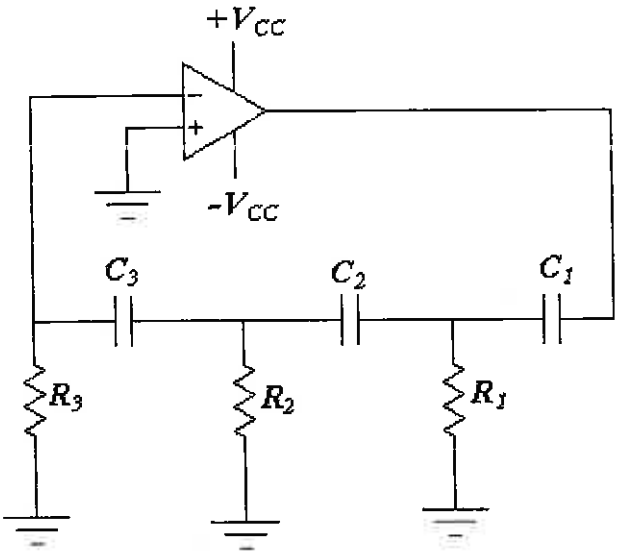

Fig. Q3[D]

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Question 4

[A] The Schmitt trigger circuit is shown in Fig.Q4 [A]. The input voltage goes from +20V to -20V. The resistances values are R_1=15kΩ and R_2 =85kΩ. Find out the positive and negative reference voltages and sketch the output waveform.

[5 Marks]

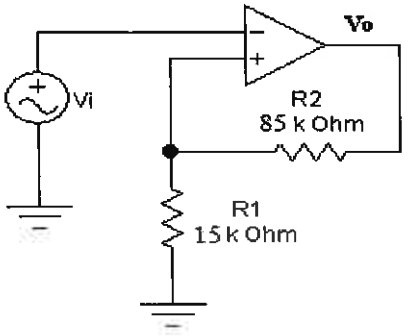

Fig. Q4 [A]

[B] Anti-logarithmic amplifier output voltage is proportional to the anti-logarithmic of the input voltage. Such an amplifier uses the non-linear volt-ampere relationship of a p-n junction. Derive an expression for the output voltage of anti-logarithmic amplifier.

[14 Marks]

[C] The anti-logarithmic amplifier circuit is shown in the Fig. Q4[C]. Determine the output voltage for the given data: I_F =0.3mA, R_3=10 kΩ, R_2 =2 kΩ, input source voltage V_S =0.1V, the silicon intrinsic standoff ratio (η) = 2 and V_T =0.026V.

[6Marks]

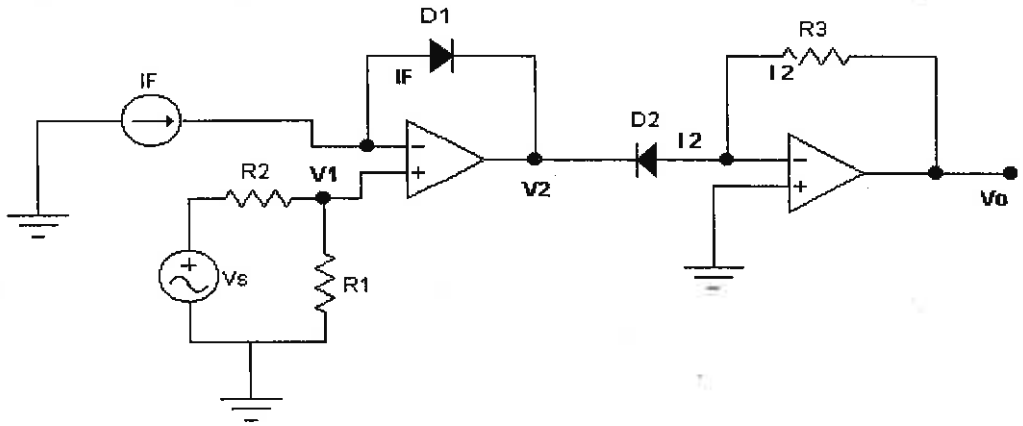

Fig.Q4[C]

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